Design and Analysis of Low Power Single Ended 8T SRAM ARRAY (4x4) at 180nm Technology

P. Raikwal
Department of E&TC
I.E.T., DAVV, Indore, INDIA
praikwal@ietdavv.edu.in

V.Neema
Department of E&TC
I.E.T., DAVV, Indore, INDIA
vneema@ietdavv.edu.in

A. Verma.
Department of E&I
I.E.T., DAVV, Indore, INDIA
averma@ietdavv.edu.in

Abstract—In embedded memories as the feature size is decreasing continuously. The demand of low power design has increased. In this paper analysis has been performed on conventional 6T SRAM cell and proposed single ended 8T SRAM cell. Here the proposed 8T SRAM cell has the advantage of low power consumption and high read static noise margin. The paper also includes SRAM cell arrays of both 6T SRAM cell and proposed single ended SRAM cell. The array comprises of address decoder, sense amplifier. The results shows that 8T SRAM array has the advantage of low power dissipation during read and write states over the array of 6T SRAM cell. The simulations are performed on Tanner EDA tool at 180nm technology.

Keywords— SRAM, Single-ended, SNM, Read static noise margin.

I. INTRODUCTION

It is well known that the SRAM consumes larger area than DRAM. Due to continuous down scaling of process technology, the integral density of the chip increases. However it led to increased power consumption [1]. Voltage scaling is a way to reduce the power consumption. Reducing the supply voltage, minimize the power consumption but it reduces the stability of the cell. Conventional 6T SRAM cell has limitation of read disturbance which is due to intrinsic voltage division between the pass transistors and pull down transistors [2]. The read stability of SRAM cell can be improved by separating the bit lines from the storing nodes. The proposed 8T SRAM cell uses single bit line. During read operation, it disconnects the bit line from the storing data nodes. Therefore, enhances the read stability of the 8T SRAM cell. In this paper the comparison of 4-bit 6T SRAM cell and 4-bit proposed 8T SRAM cell has been performed. The address decoder is used to select the particular cell to write data and to be read. Sense amplifier is used to read the stored data from the 4x4 SRAM cell array. Fig.1 show standard 6T SRAM cell.

II. PROPOSED 8T SRAM CELL

A single ended 8T static random access memory has been proposed here shown in fig. 2. It has a single bit line and two separate word lines wwl and rwl for write and read operation respectively, which enhances the write ability and read stability of the cell. The proposed cell has two cross coupled inverters, left inverter has three transistors P-2, N-1, N-2 and right inverter has two transistors P-1, and N-3. There is a signal called (CS) charge storage. During read operation CS is off which forces the stored bits at Q and Qbar not to be changed.

In the proposed cell the read and write operation are controlled by separate word lines. The write word-line (wwl) is used to transfer data from single bit-line (bl) to Q and the inverted information is stored at Qbar. When read word line
(rwl) is activated, the bit line (bl) is used to transfer data from the cell as the output during read operation. In this proposed cell, the data stored at node Q, will have to pass through the PMOS transistor, which control the read operation of the cell. When 0 is stored at node Q, PMOS_3 will be ON and while enabling RWL, the charged stored at bit line will pass through the transistors PMOS_3 and NMOS_6, and in that manner sense amplifier detect the stored 0 at Q. When 1 is stored at node Q, the connected PMOS_3 transistor will be off. That forces the bit line charge to remain constant and sense amplifier read the stored value ‘1’. In this proposed cell, the data stored at node Q, will have to pass through the PMOS transistor, which control the read operation of the cell. When 0 is stored at node Q, PMOS_3 will be ON and while enabling RWL, the charged stored at bit line will pass through the transistors PMOS_3 and NMOS_6, and in that manner sense amplifier detect the stored 0 at Q. When 1 is stored at node Q, the connected PMOS_3 transistor will be off. That forces the bit line charge to remain constant and sense amplifier read the stored value ‘1’.

Fig.2. Schematic of proposed 8T SRAM cell

III. ANALYSIS OF PARAMETERS

Analysis of proposed 8T SRAM cell in terms of write ability, read stability, hold static noise and power dissipation has been carried out in this section. These results are compared with standard 6T SRAM cell. The circuit is characterized by using the 180nm technology with the supply voltage of 1.8 volt. Circuit verification is done on the Tanner tool. Schematic of the SRAM cell is designed on the S-Edit and net list simulation done by using T-spice.

A. Read and Hold Stability

Static noise margin (SNM) is the most common approach to measure hold stability and read stability of the cell [7]. Hold stability is calculated when the cell is in hold state [3] [4]. In hold state the word lines are off, so the cell is totally disconnected from the bit lines. Read stability is measured by Read Static Noise Margin (RSNM) [5] [6]. In the proposed 8T SRAM cell due to storing nodes isolation we get better RSNM comparable to hold static noise margin (HSNM). Thus in proposed cell read stability has increased because of decoupling of bit line to the cell. Table 1 shows the SNM for read and write state.

<table>
<thead>
<tr>
<th>CELL</th>
<th>Hold SNM</th>
<th>Read SNM</th>
</tr>
</thead>
<tbody>
<tr>
<td>6T SRAM</td>
<td>640mv</td>
<td>582mv</td>
</tr>
<tr>
<td>Proposed 8T SRAM</td>
<td>681mv</td>
<td>610mv</td>
</tr>
</tbody>
</table>

Table 1: Comparison of Hold SNM and Read SNM of 6T SRAM and proposed 8T SRAM cell

B. Write Trip Point (Write Ability)

Write trip point is the measure of write ability of the cell. It shows how difficult it is to write to the storing nodes of the cell. The bit-line voltage is swept from 0 to VDD, and the flipping of the cell, when Q and Q bar flip their content is captured [3] [6]. The value of bit-line voltage at the crossing point of internal storage nodes Q and Q bar represents write trip point. Table 2 depicts write trip point of both the cells.

<table>
<thead>
<tr>
<th>CELL</th>
<th>Write trip point</th>
</tr>
</thead>
<tbody>
<tr>
<td>6T SRAM</td>
<td>576.84mv</td>
</tr>
<tr>
<td>8T SRAM</td>
<td>697.40mv</td>
</tr>
</tbody>
</table>

Table 2: Comparison for write trip point of 6T SRAM and proposed 8T SRAM cell

write ability (in mv)

Fig.3. Comparison of write trip point
C. Power Dissipation

The proposed 8T SRAM cell saves power due to single bit line. The proposed 8T SRAM cell saves 41.54% power during write ‘1’ operation and 39.78% during write ‘0’ operation. During read operation it saves 97.01% power. During hold state proposed 8T SRAM cell shows approximately same power consumption as conventional 6T SRAM cell. Table 3 shows the results.

Table 3: Comparison of power dissipation of 6T SRAM cell and proposed 8T SRAM cell

<table>
<thead>
<tr>
<th>Different modes of operation</th>
<th>Average power dissipation of 6T SRAM cell</th>
<th>Average power dissipation of proposed 8T SRAM cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write ‘1’</td>
<td>6.732e-011</td>
<td>3.935e-011</td>
</tr>
<tr>
<td>Write ‘0’</td>
<td>6.732e-011</td>
<td>4.054e-011</td>
</tr>
<tr>
<td>Read</td>
<td>2.417e-004</td>
<td>1.137e-006</td>
</tr>
<tr>
<td>Hold</td>
<td>2.290e-004</td>
<td>2.279e-004</td>
</tr>
</tbody>
</table>

IV. CONVENTIONAL 6T SRAM ARRAY (4X4)

The array includes 4 rows and 4 columns to store 4-bit. The array is formed of conventional 6T SRAM cell, which is used to store a bit. To select particular cell, row decoder is used. The row consists of 4 cells, therefore it can save 4-bit. The address decoder is formed of NAND gate. The 2:4 decoder is used to select particular row and to activate word line. Sense amplifier is used to read the data stored in any row. The 6T SRAM array (4x4) is shown in figure 4.

![Fig.4. Schematic of 6T SRAM array (4x4)](image-url)
V. PROPOSED 8T SRAM ARRAY (4X4)

The array consists of proposed 8T SRAM cell. To write or read data from the row, decoder is enabled to select particular address. The 2:4 decoder is used to select particular row and to activate word line. Here single ended sense amplifier is used to read the stored data in any row. The proposed 8T SRAM array (4x4) is shown in figure 5.

VI. RESULTS

Power dissipation of the SRAM cell, during active mode (read and write operation) is an important functional constraint in advanced technology nodes. Here the comparison of power dissipation of 4X4 array of 6T SRAM cell and the proposed 8T SRAM cell has been carried out. Table no. 4 and Fig. 6 shows the comparison during read and write operations of both the array.

Table 4: Comparison of power dissipation of 6T SRAM array and proposed 8T SRAM array

<table>
<thead>
<tr>
<th>Different modes of operation</th>
<th>Average power dissipation of 4x4 6T SRAM cell</th>
<th>Average power dissipation of proposed 4x4 8T SRAM cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write ‘1’</td>
<td>1.8241e-003</td>
<td>7.4566e-004</td>
</tr>
<tr>
<td>Write ‘0’</td>
<td>1.8244e-003</td>
<td>7.4566e-004</td>
</tr>
<tr>
<td>Read</td>
<td>9.4022e-004</td>
<td>1.8340e-004</td>
</tr>
</tbody>
</table>
VII. CONCLUSIONS

The 6T SRAM cell shows poor read stability and write ability. The proposed 8T SRAM cell uses differential word lines which enhances both read static noise margin and write margin of the cell. The comparison has been performed between 6T SRAM array and single ended 8T SRAM array. The 8T SRAM array saves 59.12% power during write ‘1’ and write ‘0’ operation. While read operation it saves 80.49% power. Finally it is observed that the proposed 8T SRAM cell has better write ability, read stability and more power efficient as compare to 6T SRAM cell.

References