Z-Scan Based Lifting Architecture For a 2-D Discrete Wavelet transform

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Abstract—It is a brief explanation of an efficient z-scan based lifting architecture for a 2-D discrete wavelet transform was introduced. It present a new algorithm of lifting steps based on flipping technique for efficient hardware architecture with the simple control path. Here the data was optimized by parallel computations of pipeline operations. It reduces the critical path to one multiplier delay for achieving 100% hardware utilization. The proposed method is repeatable and use five transposition registers. It can be folded for minimizing data path to six multipliers and eight adders without disturbing the critical path. The hardware implementation of field-programmable gate-array target indicates better efficiency.

Keywords—Discrete wavelet transform(DWT); Z-scan method; Lifting technique; flipping technique.

I. INTRODUCTION

The discrete wavelet transform was a multi resolution tool having good resolution in time and frequency domains for short duration and long durations. The DWT has higher coding efficiency, compression ratio, quality of image restoration than cosine transform and its region of interest coding makes DWT widely used in image coding. The DWT architectures which are based on convolutions and are not suitable for efficient hardware implementation. The Daubechies [2] and Sweldens [1] lifting based DWT was derived to reduce complex operation but it has the limitation of long critical path. Several new technologies have been proposed for lifting schemes [3] in which the lifting steps are modified by combining the predict and the update stages. This forms efficient pipeline architecture with critical path of one multiplier. The DWT architecture with flipping structure will decrease the critical path by avoiding multipliers from input node to computational node. This is done by flipping each computing unit with inverse of multiplier coefficient.

The 1-D DWT is having an efficient folded architecture [8] with low hardware requirement at the cost of low throughput rate. This architecture is having the critical path delay of adder and multiplier delays (T_a+T_m). The 2-D DWT design by Lai [5], [12] has a critical path delay of multiplier delay T_m and two input-two output of throughput but need 22 registers for completing the 1-D DWT. This less critical path delay was obtained by using pipelining registers in DWT but increases the complexity. Large memory is required for the flipping implementation of 2-D [11] to reduce this, the lifting technique [15] [16] is involved in it.

In this proposed method the lifting steps are implemented in parallel and in pipeline manner for reducing the critical path delay to T_m which is a simple control path. Here dual scan architecture needs N^2/2 clocks to process N×N image and five transpositions. Section II introduces the lifting scheme of 9/7 poly phase filter. Section III is new algorithm and proposed architecture. Section IV is performance analysis and comparison and conclusions in section V.

II. LIFTING SCHEME

The lifting scheme was based on spatial [14], to construct wavelet consisting of three steps split, predict and update lifting and scale normalization. It is called second generation wavelet [13] where the polyphase matrices for wavelet, filters into steps of upper and lower triangular matrices which indicate lifting steps and a diagonal matrix of scaling steps. This was based on subsampling the even and odd samples in polyphase matrix as Laurent polynomials where lifting steps [16] are performed by Lazy wavelet transform. The polyphase matrix of a 9/7 lifting filter is given as

\[ P(Z) = \begin{bmatrix} 1 & \alpha(1+z^{-1}) & 1 \\ 0 & 1 & \beta(1+z) \\ \end{bmatrix} \]

Where \( \alpha(1+z^{-1}) \) and \( \gamma(1+z^{-1}) \) are predict polynomials, \( \beta(1+z) \) and \( \delta(1+z) \) are update polynomials and K is scale normalization factor.

For 9/7 lifting filter the coefficients are \( \alpha=1.86134342, \beta=0.052980118, \gamma=0.8829110762, \delta=0.4435068522 \) and scaling coefficient is \( K=1.149604398 \).

For given sequence \( x(n) \) of \( n=0,1,\ldots,N-1 \) the lifting algorithm steps are given as

1.) Split step:

\[ d^{D}_{j}=x_{2j+1} \]
\[ s_i^0 = x_{2i} \] (3)

2.) Lifting steps

First Lifting step

\[ d_i^1 = d_i^0 + \alpha (s_i^0 + s_{i+1}^0) \] Predictor (4)

\[ s_i^1 = s_i^0 + \beta (d_i^1 + d_i^1) \] Updater (5)

Second Lifting step

\[ d_i^2 = d_i^1 + \gamma (s_i^1 + s_{i+1}^1) \] Predictor (6)

\[ s_i^2 = s_i^1 + \delta (d_i^2 + d_i^2) \] Updater (7)

3.) Scaling step

\[ d_i = \frac{1}{k} \times d_i^2 \] (8)

\[ s_i = k \times s_i^2 \] (9)

Here \( d_i \) and \( s_i \) are high pass and low pass wavelet coefficients. In this architecture the first and second lifting steps were implemented by same processor element which is in pipelined manner by feeding appropriate lifting coefficients. Here the data path of this lifting architecture was folded to improve area, efficiency at the cost of more computational cycles.

III. NEW ALGORITHM AND PROPOSED ARCHITECTURE

For the DFG shown in figure(1) the \( d_i^0 \) and \( s_i^0 \) are input data to current cycle and \( d_i^2 \) and \( s_i^2 \) are outputs of current cycle which uses the intermediate data \( d_{i+1}^0, s_{i+1}^0, d_i^1, s_i^1 \) and \( d_{i+1}^1 \) stored in internal memory devices. In the proposed algorithm the DFG was modified by processing the data in head for reducing the critical path.

\[ d_i = \frac{1}{\alpha} \cdot d_i^0 + \frac{1}{\alpha} \cdot (s_i^0 + s_{i+1}^0) \] (10)

\[ s_i^1 = \frac{1}{\alpha} \cdot s_i^0 + \frac{1}{\alpha} \cdot (d_i^1 + d_i^1) \] (11)

\[ d_i^2 = \frac{1}{\alpha} \cdot d_i^1 + \frac{1}{\alpha} \cdot (s_i^1 + s_{i+1}^1) \] (12)

\[ s_i^2 = \frac{1}{\alpha} \cdot s_i^1 + \frac{1}{\alpha} \cdot (d_i^2 + d_i^2) \] (13)

As the intermediate data was on different lifting steps they can be calculated in the same time with the current operation and used in next operation. This was stated with an example of equation (10) during the computation of \( \frac{d_i^1}{\alpha} \), \( \frac{d_i^0}{\alpha} \) is parallel computed with addition operation of \( s_i^0 \) and \( s_{i+1}^0 \) and same for equations (11). In equations (12) and (13) the first lifting steps were used so they were scaled with \( \frac{1}{\beta \gamma} \) and \( \frac{1}{\gamma \delta} \) respectively. Modified DFG was shown in figure. Now the final outputs are

\[ d_i = \alpha \beta \gamma d_i^2 \] (14)

\[ s_i = \alpha \beta \gamma \delta s_i^2 \] (15)

Here the proposed architecture minimized to the critical path delay \( T_m \) from 2\( T_m \).

B. Proposed Architecture

The dual scan [10] parallel flipping architecture is derived from proposed from modified DFG in which odd and even inputs are accessed in a Z-scan fashion as shown in Fig.2

The raising edge of clock has numbers which represents the order of pixels read. The image was divided into a tile of 2×2 pixels. The column processing would start whenever best row processed 1-D DWT was generated. The 2-D DWT was generated from the 1-D row and column processing. As the proposed 2-D architecture can be extended to 3-D by row and column processing of 2-D. Z-scan makes row and column processing [7] at the same time which results small fixed latency and transposing buffer size which is independent of N.
The lifting steps in processing element using z-scan method in [7] was shown in table II. Here the two’s compliment arithmetic operations are considered by multiplying with inverse coefficient values of $2^k$ to reduce the critical path. The equations (11), (12), (13) are scaled with constants 16, 32, 8, respectively. The equation (10) does not have any scaling factor because it has $\alpha$ more than 1.

The Z-scan data flow of row processor of PE1 can be shown in Table I, indicating the latency of five clocks for generating output. So the second input generated from preceding pipeline stage was delayed by five clocks by delay register 5D. The column PE was same as row PE but it has two outputs one is row output and other is line buffer which is at adder line [7].

This can be applied efficiently to 3-D architecture by introducing another lifting step [9]. In this the 2-D coefficients are again processed by row and column processor.

Table II

<table>
<thead>
<tr>
<th>Clk</th>
<th>D1</th>
<th>D2</th>
<th>adder</th>
<th>shifter</th>
<th>3D mul.</th>
<th>O1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$S_0^i$</td>
<td>0</td>
<td>$S_0^i + 0$</td>
<td>0</td>
<td>0</td>
<td>no</td>
</tr>
<tr>
<td>1</td>
<td>$S_1^0, N/2$</td>
<td>$S_i^0$</td>
<td>$S_i^0, N/2 + O$</td>
<td>$S_i^0 + 0$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>$S_i^0, 1$</td>
<td>$S_i^0, N/2$</td>
<td>$S_i^0, 1 + 0$</td>
<td>$S_i^0, N/2 + O$</td>
<td>$d_i^0$</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>$S_i^0, 1$</td>
<td>$S_i^0, N/2$</td>
<td>$S_i^0, 1 + S_i^0, N/2$</td>
<td>$d_i^0$</td>
<td>$d_i^0, 0$</td>
<td>$d_i^0/\alpha$</td>
</tr>
<tr>
<td>4</td>
<td>$S_i^0, 1$</td>
<td>$S_i^0, N/2$</td>
<td>$S_i^0, 1 + S_i^0, N/2$</td>
<td>$d_i^0$</td>
<td>$d_i^0, 0$</td>
<td>$d_i^0/\alpha$</td>
</tr>
<tr>
<td>5</td>
<td>$S_i^0, 1$</td>
<td>$S_i^0, N/2$</td>
<td>$S_i^0, 1 + S_i^0, N/2$</td>
<td>$d_i^0$</td>
<td>$d_i^0, 0$</td>
<td>$d_i^0/\alpha$</td>
</tr>
</tbody>
</table>

IV. PERFORMANCE ANALYSIS AND COMPARISON

The performance calculations of 2-D and 3-D 9/7 DWT architecture with previous architectures was evaluated in Tables II. 1-D processor has eight adders and four multipliers having 20 delay registers. The proposed method has critical path delay of $T_m$ having throughput of two outputs per cycle with $N^2/2$ computational cycles to process the image with $N x N$.

Here the precalculation are regular so the design can easily be folded for the data path having two adders and one multiplier without interfering with critical path. The optimized lifting technique stated in [4] has same critical path, but it need $N^2$ clock cycles. In that it is also shown that 1-D technique has better throughput but it has more computational cycles. In the present 3-D method uses twelve multipliers in which, ten for PE and two for scaling in each PE and for 2-D ten multipliers among eight for PE and for scaling. As two adders where used in each PE, which results 16 adders for complete 2-D processing. Here the proposed method can be folded, only six multipliers and eight adders are used without disturbing the critical path.

The high-speed architecture proposed in [6] has higher throughput than proposed method but is having long critical path because of reusing of single hardware unit for predict and update purpose.
V. CONCLUSIONS

Here the new Z-scan based lifting architecture for 2-D and 3-D discrete wavelet transform of 9/7 filter was proposed. The efficient lifting technique has critical path delay of $T_m$ and throughput of two outputs per cycle. In this the proposed method was compared with traditional lifting techniques in terms of hardware complexity, critical path delay, memory size and throughput. It is concluded present technique has high speed architecture of symmetrical low hardware complexity. The simulation results of 2-D and 3-D DWT at different intensity values are shown.

References