A 12 Bit 50MSPS Low Power SAR ADC in UMC 65nm Technology

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Abstract - The use of analog to digital converters (ADCs) is becoming well established in frequency domain applications such as radar and wireless receivers. The boundary between analog and digital signal processing is moving closer to the antenna. So for analog-to-digital converters (ADCs) of radio receivers this indicates higher sample rate, higher resolution, and lower power dissipation. The wireless receiver architectures, showing the greatest potential to meet the commercial trends, include the direct conversion receiver and the super heterodyne receiver with an ADC sampling at the intermediate frequency (IF). The SAR ADC architecture, based on the switched capacitor (SC) technique, has most successfully covered the widely separated resolution and sample rate requirements of these receiver architectures. A 12-bit resolution is chosen considering the dynamic range of input signal. To avoid common-mode errors, the SAR ADC uses a differential topology. To decrease area, power and cost while maintaining 12-bit accuracy, the Binary-Weighted (BW) capacitor array is split into two sub-BW capacitor arrays. A dynamic latch discriminates voltage differences as small as 100 V while concurrently working with rail-to-rail input signals. A uni-directional switching technique is introduced to minimize the dynamic power. The SAR ADC is designed with UMC 65nm CMOS technology.

Keywords - ADC, SAR, SC, BW Capacitor Array, Split Capacitor Array, Unidirectional Switching.

I. INTRODUCTION

The increasing demands of telecommunication systems are continuously demanding high performance integrated circuits. Analog interface circuits may be negatively affected by technology scaling but digital processing can exploit the improvements introduced by deep submicron technologies. In particular, power supply scaling and intrinsic transistor gain reduction significantly influence the design of high performance analog components. So a mixed signal design approach is suitable for high speed ADC design. Wireless communications have been the driving force in analog electronics development during the last decade. As the end products are produced for every-day use, the price, size, and weight of the devices play a large part in determining their design. Cost reduction and miniaturization require higher integration levels, while battery lifetime is one of the most critical parameters for the user of hand-held equipment requiring low power. At the same time wireless communication standards, like the Universal Mobile Telecommunication System (UMTS), Wireless Local Area Network (WLAN) and Wireless Local Loop (WLL) are evolving towards higher data rates, thus allowing more services to be provided. The design is still mostly performance oriented.

The continuously growing complexity of the modulation schemes and the desire for more flexible receivers push the boundary between analog and digital signal processing closer to the antenna, thus aiming for a software defined radio. These two trends set the specifications of the analog-to-digital converter (ADC) in a radio receiver.

As the ADC to be integrated in a system on chip (SOC) receiver the power consumption must be low. Generally in satellite or RF communication the received signal has a dynamic range of 60dB. So in receiver architecture no component should have SNR value less than 60dB. So for ADC also output SNR should be more than 60dB. Now in order to achieve a output SNR of 60dB the effective number of bits (ENOB) of the ADC should be 10 Bit. To get a ENOB of 10 Bit a 11 or 12 Bit architecture should be chosen, as manufactured ADC will not work as ideal one. It is better choose slight over specification giving relaxation to layout and manufacturing process instead of stringent design and manufacturing process. As the ADC is going to be used in voice receiver circuit the static performance of the ADC can be relaxed. But in order to avoid any missing code the DNL of the ADC should be less than 1 LSB. Now for given receiver architecture the input signal bandwidth is 5 MHz so the sampling speed of the ADC should be more than nyquist rate i.e. 10 MSPS. But in order to relax the base band filter requirement an oversampling ADC is suitable. So a sampling rate of 50 MSPS is chosen. So by taking a little extra
specification than required we can specify the requirement for ADC. Analog to Digital Converter (ADC), is an electronic circuit that converts continuous analog signals into discrete values. An analog signal needs to be quantized in order to be converted in a digital one. An analog signal can take infinite values; quantization consists in the substitution of these infinite values into discrete and finite amounts of values.

In the simple implementation Flash (parallel) ADC is the fastest type of converter but, has limited resolution, high power dissipation[1]. SAR ADC topology is expected to allow the lowest power dissipation, but paying the price with the slowest sampling rate[2]. The linearity of the A/D converter is not affected by the comparator offset voltage [3]. The monotonic capacitor switching procedure explained [4], has more power dissipation even in pipelined SAR ADC[5-6]. However in reality the effective resolution lower than N bits due to different error sources[7-9], comparative study between works of capacitor less LDO voltage regulators with different pass devices[10-14] the advantage disadvantages of each pass device were identified and its study depend.

The design of a 12-bit, 50 MSPS low power SAR ADC in UMC 65 nm CMOS technology consumes a total power of 0.68 mW using a large unit capacitance of 0 to 100 fF. Section II presents proposed architecture of SAR ADC, the measured and simulation results are presented in Section III. Conclusions are given in Section IV.

II. ARCHITECTURES OF SAR ADC

Flash ADC is the fastest type of converter, but has limited resolution, high power dissipation [1]. Successive approximation ADC with in encode and a comparator consumes low power but having poor sampling rate[2]. Fig.1 illustrates the block diagram of a SAR ADC including a sample and hold circuit which is a common architecture for SAR ADC. In this configuration, the capacitor offset voltage can be modeled as a voltage source in series combination with the output of the sample-and-hold circuit which implies the addition of the offset to the analog input. As a result, an offset appears in the overall characteristic. Therefore, the linearity of the A/D converter is not affected by the comparator offset voltage [3]. The drawback of this approach is that it consumes high power due to separate S/H circuit.

(i) Charge Redistribution Architecture

As pipelined ADC consuming more power[5-6]. This architecture encompasses a capacitive DAC which also operates as a sample and hold. The block diagram of the charge redistribution SAR ADC is illustrated in Fig. 2. The D/A converter usually contain a binary weighted capacitor array. In each conversion, first the analog input is sampled and stored in the capacitor array and then the output of the DAC is compared to VCM for N clock cycle. The output of the DAC successively follows the VCM voltage at the comparator’s input and reaches VCM at the end of each conversion.

![SAR ADC with capacitive DAC](image)

The main advantage of this configuration is its low power consumption due to inherent sample-and-hold operation inside the capacitive DAC.

(ii) Proposed SAR ADC core

The proposed SAR ADC uses a unidirectional switching method [7-9] to reduce switching power in each conversion. The conventional switching process is given in Fig. 3 and the unidirectional switching process is shown in Fig. 4. In conventional switching procedure at the sampling phase, the bottom plates of the capacitors are charged to Vip, and the top plates are reset to the common-mode voltage Vcm. Next, the largest capacitor is switched to Vref and the other capacitors are switched to ground. The comparator then performs the first comparison. If is higher than, the most significant bit (MSB) is 1. Otherwise, is 0, and the largest capacitor is reconnected to ground. Then, the second largest capacitor is switched to Vref. The comparator does the comparison again. The ADC repeats this procedure until the least significant bit (LSB) is decided. Although the trial and error search procedure is simple and intuitive, it is not an energy efficient switching scheme, especially when unsuccessful trials occur.

In proposed SAR ADC, where the proposed switching procedure can be either upward or downward. For fast reference settling, i.e., discharging through n-type transistors, downward switching was selected in this ADC. The proposed ADC samples the input signal on the top plates via bootstrapped switches. At the same time, the bottom plates
of the capacitors are reset to $V_{\text{ref}}$. Next, after the ADC turns off the bootstrapped switches, the comparator directly performs the first comparison without switching any capacitor. According to the comparator output, the largest capacitor on the higher voltage potential side is switched to ground and the other one (on the lower side) remains unchanged. The ADC repeats the procedure until the LSB is decided. For each bit cycle, there is only one capacitor switch, which reduces both charge transfer in the capacitive DAC network and the transitions of the control circuit and switch buffer, resulting in smaller power dissipation.

One of the major differences between the proposed method and the conventional one is that the common-mode voltage of the reference DAC gradually decreases from half $V_{\text{ref}}$ to ground as shown in Fig. 4. The proposed switching sequence does not require upward transition. At the same transistor size, the on-resistance of a nMOS switch is only about 1/3 that of a pMOS one. Having no upward transition speeds up the DAC settling. In addition, since sampling is done on the top plate, the comparator can do the first comparison without any capacitor switching. The switching waveform for one conversion of conventional SAR and proposed SAR ADC are shown in Fig. 5 and Fig.6 respectively.
A/D Converter contains at least one comparator. A comparator itself can be considered a 1-bit A/D Converter. For 12 bit ADC with Vref as 1.2V the comparator must be able to discriminate voltage as small as 146.48 μV (.5VLSB= 146.4 μV). Comparators design must consider Offset voltage, Resolution, Speed, Bias current, Power dissipation.

The comparator is the block that affects the most the total power consumption of the SAR ADC. It is generally composed by preamplifiers and latch. But our aim is to make a low power ADC. For our required speed of 50 MSPS with 12 bit accuracy, the comparator has to take decision 12 times in 20 ns. So approximation response time of preamplifier should be less than 1ns. For such less response time the bandwidth requirement of the amplifiers will be in GHz. To achieve this bias current requirement will be too high. Also a preamplifier requires a offset correction logic in each cycle after each comparator decision. Offset correction at such speed is also a very difficult. For this architecture a dynamic comparator is used .Dynamic comparators are Latch type sense amplifiers. They are high energy effective comparators as they do not require continuous biasing current. They can achieve fast decisions due to a strong positive feedback. During the conversion phase, the input voltages of the comparator approach ground. For proper function within the input common mode voltage range from half to ground, the comparator uses a p-type input pair. Because a dynamic comparator does not consume static current, it is suitable for energy efficient design.

When clock is high, the comparator outputs, outp and outm are reset to high. When goes to low, the differential pair PM0 and PM1 compares the two input voltages. Then, the latch regeneration forces one output to high and the other to low according the comparison result. Consequently, the valid signal is pulled to high to enable the asynchronous control clock.

The offset voltage of this comparator can be expressed as

\[ V_{OS} = V_{TH,1,2} + \frac{(V_{GS} - V_{TH})_{1,2}}{2} \left( \frac{\Delta S_{1,2} R}{\Delta R} + \frac{\Delta R}{R} \right) \]  

(1)

Where \( V_{TH,1,2} \) is the threshold voltage offset of the differential pair PM0 and PM1 . \( (V_{GS} - V_{TH})_{1,2} \) is the effective voltage of the input pair, \( VV_{TH,1,2} \) is the physical dimension mismatch between PM0 and PM1, and \( R \) is the loading resistance mismatch induced by NM5–NM6.

The first term is a static offset which does not affect the performance of a SAR ADC. However, the second term is a signal-dependent dynamic offset. The effective voltage of the input pair varies with the input common-mode voltage.

There are several possible approaches to improve the dynamic offset. The comparator size can be enlarged, which results in larger power consumption. The effective voltage of the input pair can be reduced, but this decreases the comparison speed. A simple and reliable way is to cascade a biased MOS (PM5) at the top of the switch MOS (PM4). Because PM5 is in the saturation region, the change of its drain-source voltage has only a slight influence on the drain current. Hence, PM5 keeps the effective voltage of the input pair near a constant value when common-mode voltage changes. The dynamic offset thus has a minor influence on the conversion linearity. But still both the outputs are always changing to One when the comparator is in resting phase i.e. clock is high. So switching energy is more due to change in output value in each clock cycle. So in order to avoid output transition comparator can be modified further.

Digital-to-Analog Converter (DAC)

A common implementation of switch cap SAR ADCs uses a binary-weighted capacitor array. For binary-weighted capacitor arrays, however, area and power increase exponentially with resolution. In fact, n bit resolution requires 2^n unit capacitors. Split capacitor arrays as well as C-2C ladders reduce the total capacitance, thereby reducing area and power. However, the parasitic bottom-plate capacitance of series capacitors affects the linearity of the ADC. So a in order to avoid the problems in binary-weighted capacitor array and C-2C ladders capacitor array a intermediate solution is considered i.e. a Two Sub Binary Weighted Capacitor array. Two Sub Binary Weighted Capacitor array consists of two stages of capacitive DAC and connected by bridge capacitor. The capacitors in each stage are multiplier of a unit capacitor. The unit capacitor value calculated from total KT/C noise value offered by capacitors.

\[ SNR = 10 \log \left( \frac{A^2}{12} \right) - \frac{\Delta^2}{12} - N_{thermal} \]  

(2)
Where $A$ is input signal amplitude, $\frac{\Delta^2}{12}$ is the Quantization noise and $N_{\text{thermal}}$ is the thermal noise or KT/C noise.

So from our SNR requirement the unit capacitor value from equation is calculated to be 20 pF but considering the matching requirement and minimum MIM (metal insulator metal) capacitor available by the technology, the unit capacitor is chosen to be 50 fF.

Two sub binary weighted capacitor array is used to implement a differential architecture. As a fully differential analog signal path has several advantages with respect to a single-ended analog signal path.

The buffer switches used to connect the capacitor bottom plate to $V_{\text{ref}}$ or ground also plays important role in DAC settling. The settling time of capacitive circuit is depends on $R$-C time constant. As per our requirement we have fixed the capacitor size in DAC, now for proper settling of DAC value in required time frame the sizing of buffer switch for each capacitor is necessary. As capacitors in DAC are scaled down by two we can also scale down the first buffer switch and use it for consecutive capacitors. The control signal for switches is generated by the SAR control logic. use it for consecutive capacitors. The control signal for switches is generated by the SAR control logic.

(v) Successive Approximation Register (SAR)

Successive approximation register (SAR) ADC implements the binary search algorithm using SAR control logic. The Successive Approximation Register sets the switches as a function of the current state of the conversion and the comparator’s response and stores the digital output code to be issued at the end of the conversion. For a high-speed operation, the SAR logic must be well designed to achieve more spare time allocation for the settling of DAC. Meanwhile, in order to reduce the power consumption, the digital part should be simplified. To avoid using a high-frequency clock generator, the proposed ADC uses an synchronous control circuit to internally generate the necessary clock signals. The proposed SAR control logic is given in the Fig. 7. The SAR logic is constitutes of two rows of D flip flop (DFF) and switch control logic. The first rows of DFFs, as shown in Fig. 8, are used to generate a set of asynchronous clock to control the switches at edge of these clock signals. The generated asynchronous Control signals are shown in Fig. 8. The asynchronous control signals generated from first row DFFs are now acting as clock for second row DFFs. So as shown in Fig. 11 at rising edge of these asynchronous clocks the reconfiguration of switches are taking place.

The proposed SAR ADC takes 14 clock cycles for each conversion. So the start signal is of 14 clock cycle.

START signal is given to ADC from outside. It is user control Signal. The First two clock cycles period of START is reserved for Sampling of and rest 12 clock cycle for conversion of sampled data. While conversion of data the remaining 12 cycle, the comparator takes decision in negative half of clock cycle and SAR logic switches the switch buffers on positive clock cycle.

(vi) Sample and Hold Stage (S/H)

In our SAR ADC we choose to use the capacitor array as sampling capacitor to acquire the analog signal during the sampling phase. The sampling phase is taken as two clock cycle to ensure the data is correctly sampled to the DAC. Now in order to sample the data we need a switch circuit. We can use a Transmission Gate (TG) or bootstrapped switch as the sampling switch. The switch linearity should be more than that of ADC. In other terms the SNR of the switch should be more than our ADC output SNR. If the TG with dummy transistors used the charge injected from that switch onto the capacitor array is high enough to make the A/D conversion fail. So the idea is to use a bootstrapped switch with constant $V_{\text{GS}}$, so that the channel resistance of the switch remains constant and it will have a greater linearity. Also If $V_{\text{Gs}}$ is constant, then the channel charge is constant, as $Q_{\text{eh}} = WLC_{\text{ox}} (V_{\text{GS}} - V_{\text{tm}})$ with the fully differential topology, the same amount of charge would be injected onto both capacitor arrays, whatever the signal level, and the effect would be cancelled out.
III. SIMULATION RESULTS

Transient simulations
To test the ADC core, the A/D conversions listed in Table 1 have been simulated. The designed ADC able to generate the correct digital code for given input signal.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Expected code</th>
<th>Simulated output code</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2V</td>
<td>111,111,111,111</td>
<td>111,111,111,111</td>
</tr>
<tr>
<td>0V</td>
<td>000,000,000,000</td>
<td>000,000,000,000</td>
</tr>
<tr>
<td>0.9V</td>
<td>110,000,000,000 or 101,111,111,111</td>
<td>101,111,111,111</td>
</tr>
<tr>
<td>0.6V</td>
<td>100,000,000,000 or 011,111,111,111</td>
<td>100,000,000,000</td>
</tr>
<tr>
<td>0.3V</td>
<td>010,000,000,000 or 001,111,111,111</td>
<td>010,000,000,000</td>
</tr>
</tbody>
</table>

The transient wave results are given below for various input (1.2V, 0V, 900mV, 600mV and 300mV).
**Power and Current Consideration**

Several simulations are performed in order to check the current flowing through the whole circuit and how it is divided between the different blocks. The current is directly proportional to the power consumption, so we can estimate it. The analog part, including the S/H circuit and comparator consumes a 400 W of power. These two are the highest power consuming block on ADC. The DAC consumes a dynamic power of 150 W and SAR logic consumes a dynamic power of 130 W. So the total power consumed by the SAR ADC is 680 W.

**Comparison with the Previous works**

Table 2 shows the performance comparison of the proposed work with respect to the recent prior-art works of capacitor less LDO[10-14]. It indicates that the optimal trade-off performance can be obtained in the proposed work.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>[10]</th>
<th>[11]</th>
<th>[12]</th>
<th>[13]</th>
<th>[14]</th>
<th><strong>This work</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Tech.[µm]</td>
<td>0.35</td>
<td>0.38</td>
<td>0.35</td>
<td>0.11</td>
<td>0.18</td>
<td>0.13</td>
</tr>
<tr>
<td>Vin[VPp]</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Cout[PF]</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>40</td>
<td>100</td>
<td>0-100</td>
</tr>
<tr>
<td>Cm[PF]</td>
<td>3</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>8</td>
</tr>
<tr>
<td>Imax[MA]</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>200</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Iq[µA]</td>
<td>27-270</td>
<td>14-53.5</td>
<td>7</td>
<td>41.5</td>
<td>3.7</td>
<td>50</td>
</tr>
<tr>
<td>Vout[mV]</td>
<td>N.A</td>
<td>&lt;339</td>
<td>236</td>
<td>385</td>
<td>277</td>
<td>120</td>
</tr>
</tbody>
</table>

To compare the proposed ADC to other works with different sampling rates and resolutions, the well-known Figure-of-merit (FOM) equation is used,

\[
FOM = \frac{\text{Power}}{2 \times \text{ENOB} \times 2^*F_S}
\]

Where \(F_S\) is the sampling frequency i.e. 50MHz. The FOM of the proposed ADC is 17 fJ/conversion-step at 50 MS/s and a 1.2 V supply. The result comparison with other works is presented in Table 3. The proposed ADC demonstrates better result than compared works.

**IV. CONCLUSION**

A 50 MSPS low power SAR ADC is designed in UMC 65nm technology. An efficient capacitor switching procedure for SAR ADCs was presented in this report. The unidirectional switching procedure leads to both lower switching energy and smaller total capacitance. It also simplifies the digital logic control circuit. The ADC core is composed of comparator, DAC, SAR control logic and S/H circuit. These components have been designed targeting to fulfill several constraints on requirements such as the offsets due to mismatch and low power consumption. The ADC achieves a 50-MS/s operation speed with power consumption of less than 700 uW. The desired dynamic performance is achieved.

**REFERENCES**


